# Sub Code: 18BIT46S

## Skill Based Subject – II: MICRO PROCESSOR & ASSEMBLY LANGUAGE PROGRAMMING

**UNIT V:** I/O ports- Programmable Peripheral interface - Architecture of Intel 8255-Programmable DMA controller - Programmable interrupt controller 8259 - Programmable communication interface 8251.

**TEXT BOOK**

1. B.RAM, “Fundamentals of Microprocessors and Microcontrollers”, Dhanpat Rai Publications, 7$^{th}$Edition, 2010.

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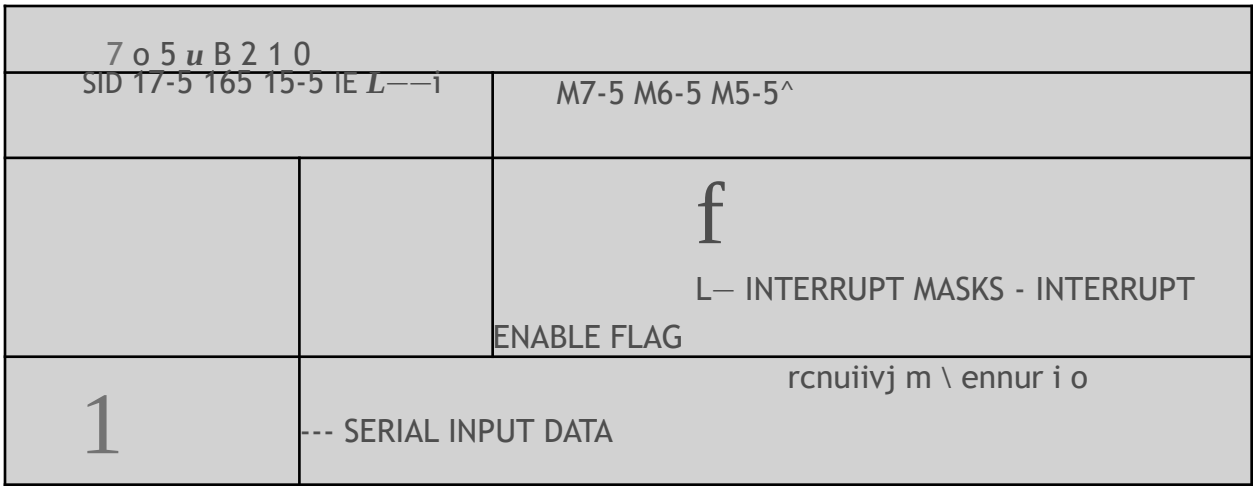
be recognized by microprocessor. To enable It again they must be unmasked (enabled) by using EI.

**4.5. Interfacing Devices and I/O Devices**

To communicate with the outside worls microcomputers use peripherals(I/O Devices). Commonly used peripherals are

- A/D converter
- D/A converter
- CRT
- Printers
- Hard disks
- Floppy disks
- Magnetic tapes

Peripherals are connected to the microcomputer through the electronic circuits known as interfacing circuits.




4.6 . Accumulator content after the execution of

RIM Some of the general purpose devices are:

i. I/O port
ii. Programmable Peripheral Interface(PPI)
iii. DMA controller
iv. Interrupt controller
v. Communication interface
vi. Programmable Counter/Interval Timer

Special purpose interfacing devices are designed to interface a particular type of I/O device to the microprocessor. Examples of such devices are:

i. CRT controller
ii. Floppy Disk Controller
iii. Key Board and Display Interface.

### 4.5.1. Generation of control signals for memory and I/O devices

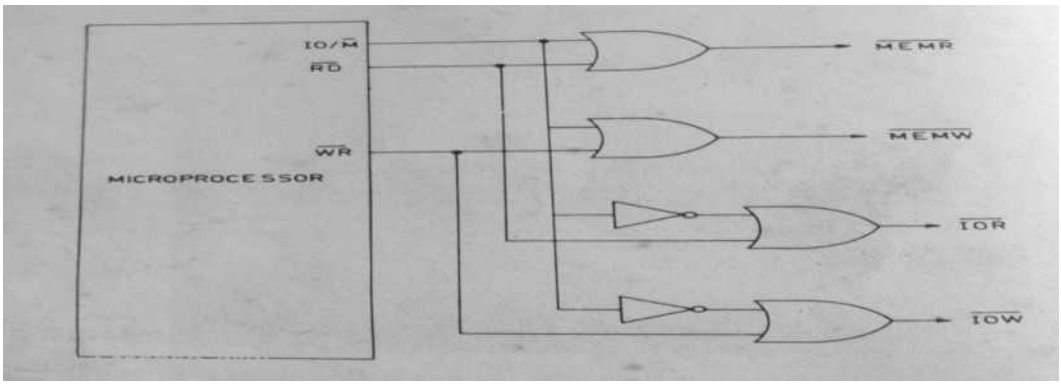
The Mp provides RD and WR signals to initiate read and write cycle. Because these signals are used both for reading / writing memory or reading writing an input/output device, it is necessary to generate separate read and write signals for memory and I/O devices. 8085 provides IO/M signal to indicate that initiated cycle is for I/O device or for memory device. Using IO/M signal along with RD and WR, it is possible to generate four signals shown below.

MEMR- Memory read

MEMW- Memory write

IOR- I/O read

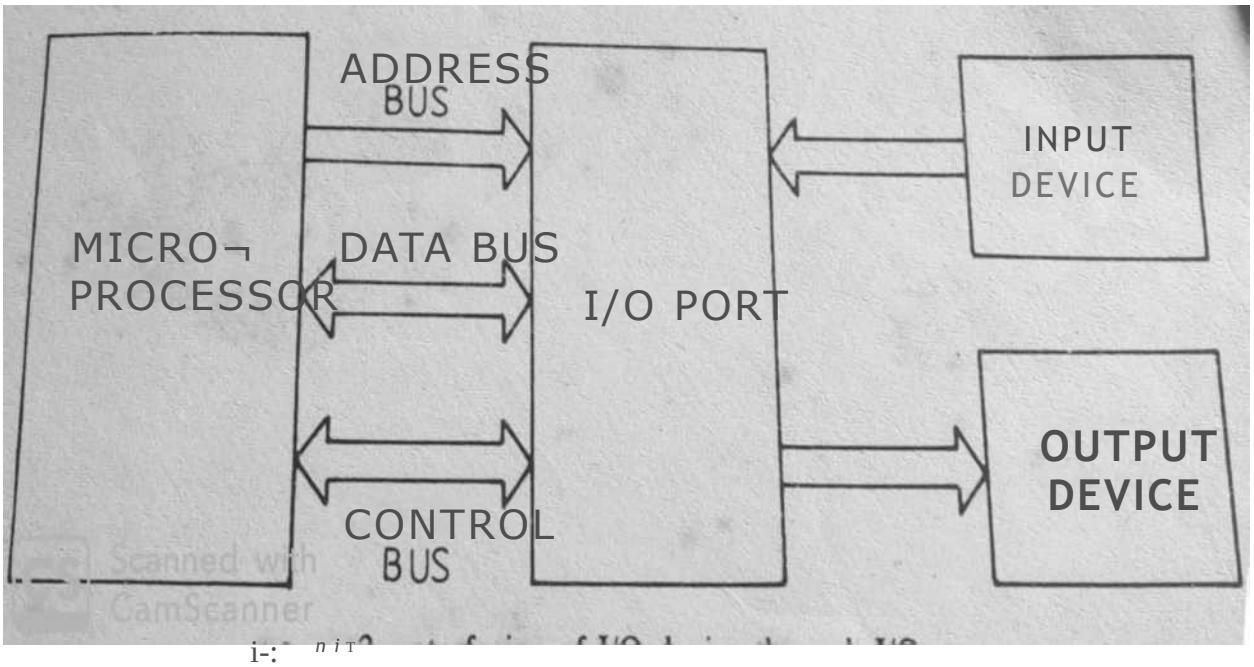
IOW- I/O write




4.7. Control signals for Mmeory I/O Read/Write Operation

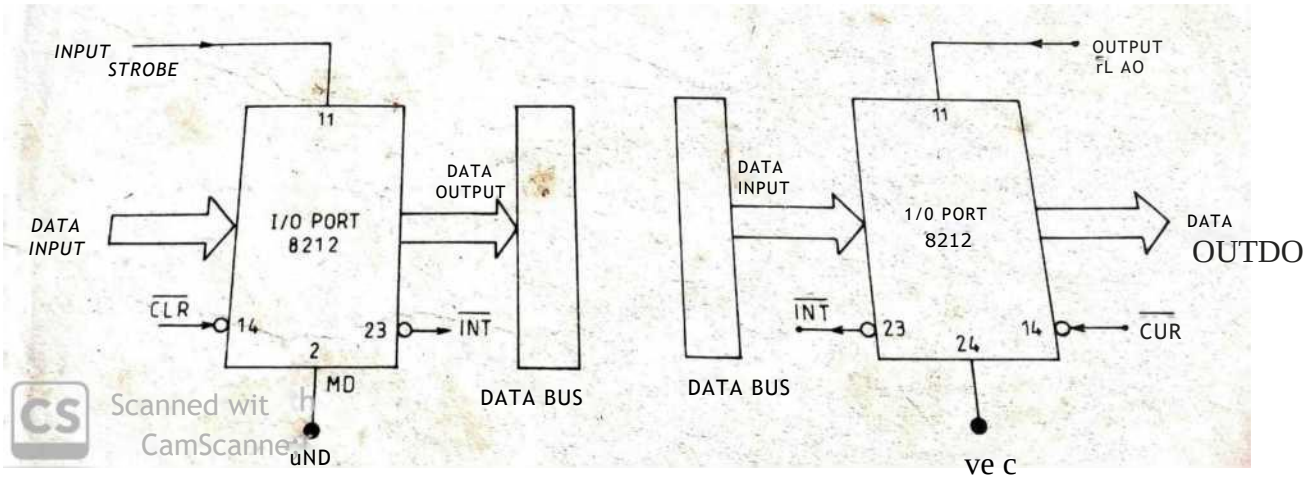
### 4.6. I/O Ports

An input device is connected to the microprocessor through an input port. An input port is a place for unloading data. An input device unloads data into the port. The microprocessor reads data from the input port. Similarly, an output device is connected to the microprocessor through an output port. As the output port is connected to the output device , data transferred to the output device.




4.8. Interfacing of I/O device through I/O port

The Intel 8212 is an 8-bit nonprogrammable I/O port. It can be connected to the microprocessor either as an input port or an output port. If we require one input port and one output port, two units of 8212 will be required. One of them will be connected in input mode and other in output mode.




(a) Input mode (b) Output Mode

4.9. Interfacing of Intel 8212

The SCL 6532 is a RAM, I/O, Interval Timer Device(RIOT) manufactured semiconductor Complex LTD. It has an 8-bit bidirectional data bus, 12x8 state R two 8-bit bidirectional data ports.

It operates with 1 MHz and 2 MHz clock and single supply +5V implemented in a 40-pin IC. It has been designed to operate in conjunction with the SCL microprocessor family. SCL 6502 is also manufactured by semiconductor Complex Ltd.

### 4.6.1. Programmable peripheral Interface (PPI).

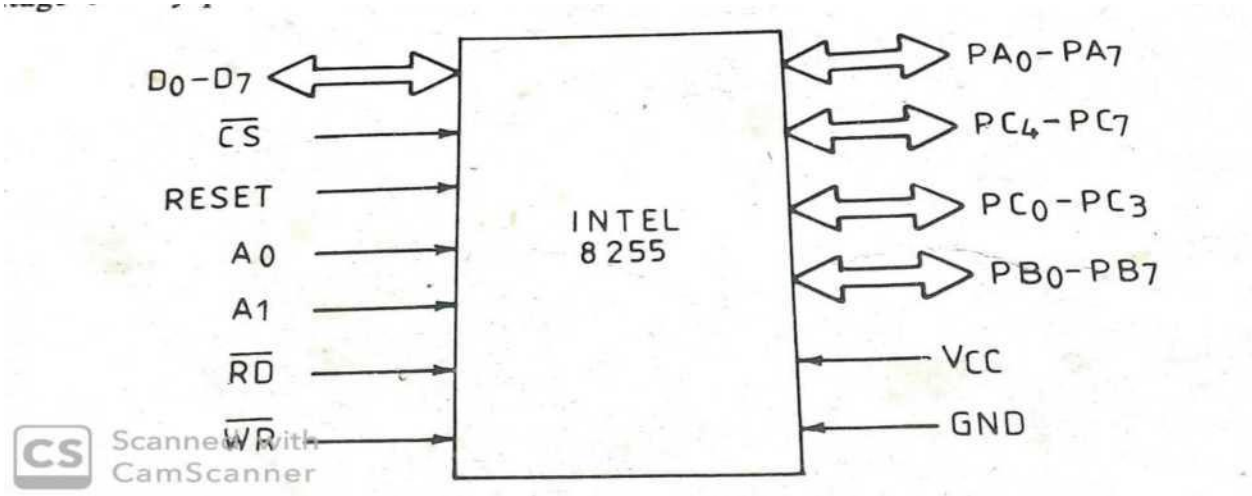
A programmable peripheral interface is a multiport device. The ports may be programmed in a variety of ways as required by the programmer. The device is very useful for interfacing peripheral devices. The term IA, Peripheral Interface Adapter is also used by some manufacturer.

PPI 8255 is a general purpose programmable I/O device designed to interface the CPU with its outside world such as ADC, DAC, keyboard etc. We can program it according to the given condition. It can be used with almost any microprocessor. It consists of three 8-bit bidirectional I/O ports i.e. PORT A, PORT B and PORT C. We can assign different ports as input or output functions.

### 4.6.2. Architecture of Intel 8255A.

**Data Bus Buffer**

It is a tri-state 8-bit buffer, which is used to interface the microprocessor to the system data bus. Data is transmitted or received by the buffer as per the instructions by the CPU. Control words and status information is also transferred using this bus.





4.10. Schematic Diagram of Intel 8255A

**Read/Write Control Logic**

This block is responsible for controlling the internal/external transfer of data/control/status word. It accepts the input from the CPU address and control buses, and in turn issues command to both the control groups.

**CS**

It stands for Chip Select. A LOW on this input selects the chip and enables the communication between the 8255A and the CPU. It is connected to the decoded address, and A0 & A1 are connected to the microprocessor address lines.

**WR**

It stands for write. This control signal enables the write operation. When this signal goes low, the microprocessor writes into a selected I/O port or control register.

**RESET**

This is an active high signal. It clears the control register and sets all ports in the input mode.

**RD**

It stands for Read. This control signal enables the Read operation. When the signal is low, the microprocessor reads the data from the selected I/O port of the 8255.

**A0 and A1 ( Address pins )**

These pins in conjunction with RD and WR pins control the selection of one of the 3 ports. Group A and Group B controls receive control from the CPU and issues commands to their respective ports.

Port A: This has an 8 bit latched/buffered O/P and 8 bit input latch. It can be programmed in 3 modes - mode 0, mode 1, mode 2.

Port B: This has an 8 bit latched / buffered O/P and 8 bit input latch. It can be programmed in mode 0, mode1.

Port C : This has an 8 bit latched input buffer and 8 bit output latched/buffer. This port can be divided into two 4 bit ports and can be used as control signals for port A and port B. it can be programmed in mode 0.

**Operating modes of 8255:**

These are two basic modes of operation of 8255. I/O mode and Bit Set-Reset mode (BSR). In I/O mode, the 8255 ports work as programmable I/O ports, while in BSR mode only port C (PC0-PC7) can be used to set or reset its individual port bits.

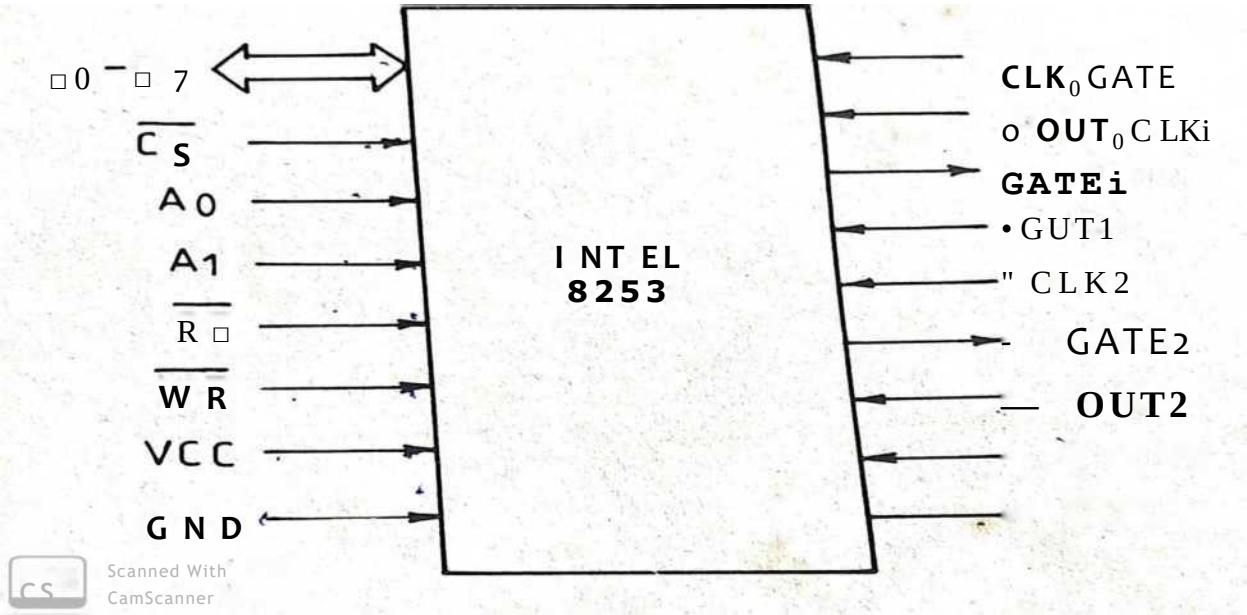
Under the I/O mode of operation, further there are three modes of operation of 8255, so as to support different types of applications, mode 0, mode 1 and mode 2.

**Mode 0 ( Basic I/O mode ):** This mode is also called as basic input/output mode. This mode provides simple input and output capabilities using each of the three ports. Data can be simply read from and written to the input and output ports respectively, after appropriate initialization.

**Mode 1: ( Strobed input/output mode )** In this mode the handshaking control the input and output action of the specified port. Port C lines PC0-PC2, provide strobe or handshake lines for port B. This group which includes port B and PC0-PC2 is called as group B for Strobed data input/output. Port C lines PC3-PC5 provide strobe lines for port A. This group including port A and PC3-PC5 from group A. Thus port C is utilized for generating handshake signals.

**Mode 2 ( Strobed bidirectional I/O ):** This mode of operation of 8255 is also called as strobed bidirectional I/O. This mode of operation provides 8255 with an additional features for communicating with a peripheral device on an 8-bit data bus. Handshaking signals are provided to maintain proper data flow and synchronization between the data transmitter and receiver. The interrupt generation and other functions are similar to mode 1.

**Intel 8253**




4.11. Schematic Diagram Of Intel 8253

**Data Bus Buffer**

It is a tri-state, bi-directional, 8-bit buffer, which is used to interface the 8253/54 to the system data bus. It has three basic functions are Programming the modes of 8253/54, Loading the count registers, Reading the count values.

**Read/Write Logic**

It includes 5 signals, i.e. RD, WR, CS, and the address lines A0 & A1. In the peripheral I/O mode, the RD and WR signals are connected to IOR and IOW, respectively. In the memory mapped I/O mode, these are connected to MEMR and MEMW.

Address lines A0 & A1 of the CPU are connected to lines A0 and A1 of the 8253/54, and CS is tied to a decoded address. The control word register and counters are selected according to the signals on lines A0 & A1.

**Control Word Register**

This register is accessed when lines A0 & A1 are at logic 1. It is used to write a command word, which specifies the counter to be used, its mode, and either a read or write operation.

**MODE 0 Interrupt on terminal count:**

In this mode, the output is initially low after the mode is set. The counter starts decrementing the count value after the falling edge of the clock till the terminal count is reached. When the terminal count is reached, the output goes high and remains high until the selected control word register or the corresponding count register is reloaded. This high output may be used to interrupt the processor. The GATE signal should be high for normal counting and When GATE goes low counting is terminated.

**MODE 1 Programmable one-shot :**

The gate input is used as trigger input in this mode of operation. Normally the output remains high. After the application of the trigger, the output goes low and remains low until the count becomes zero.

**MODE 2 Rate generator:**

The output is normally high after initialization. If GATE goes high, the counter starts counting down from the initial value. In this mode, if N is loaded as the count value, then, after N pulses, the output becomes low only for one clock cycle. The count N is reloaded and again the output becomes high and remains high for N clock pulses.

**MODE 3 Square wave generator:**

When the count N loaded is even, then for half of the count, the output remains high and for the remaining half, it remains low. If the count N loaded is odd, then for (N+1)/2 pulses the output remains high and for (N-1)/2 pulses it remains low. This procedure is repeated continuously resulting in the generation of a square wave.

**MODE 4 Software triggered strobe:**

After the mode is set, the output goes high. On terminal count, the output goes low for one clock cycle, and then it again goes high. The GATE input when low disables the counting and when high, enables the counting. The difference between Mode 4 and Mode 2 is that in Mode 2, the OUT pulses are generated continuously after every N clock pulses, but in Mode 4, the OUT pulse is generated only once after N clock pulses.

**MODE 5 Hardware triggered strobe**

The output is initially high. The counter starts counting after the rising edge of the trigger input (GATE). The output goes low for one clock period when the terminal count is reached. The hardware circuit should trigger the GATE input to initiate the counting operation, thereby generating the OUT pulse.

# Programmable interrupt controller (PIC) 8259

In computing, a **programmable interrupt controller** (**PIC**) is an integrated circuit that helps a microprocessor to (or CPU) handle **interrupt** requests (IRQ) coming from multiple different sources (like external I/O devices) which may occur simultaneously.

8259 microprocessor is defined as Programmable Interrupt Controller (PIC) microprocessor. There are 5 hardware interrupts in 8085. But by connecting 8259 with CPU, we can increase the interrupt handling capability.

# Programmable communication interface 8251

A USART (Universal Synchronous / Asynchronous Receiver / Transmitter) is also called a **programmable communications interface** (PCI). When information is to be sent by 8085 /8086 over long distances, it is economical to send it on a single line. The microprocessor has to convert parallel data to serial data and then output it. Thus lot of microprocessor time is required for such a conversion.

Review Questions

1. Explain what is (a) Memory Mapped I/O Scheme, (b) I/O Mapped I/O Scheme.
2. What are the various schemes of data transfer from CPU/memory to I/O devices and vice-versa? Discuss interrupt driven data transfer scheme with suitable example.
3. Explain in detail about DMA data transfer scheme.
4. What is interrupt? Explain enabling, disabling and masking of interrupts.
5. Explain what is vectored input and device polling.
6. Explain in detail about hardware and software interrupts.
7. What are I/O ports? What are programmable and nonprogrammable ports?
8. Explain in detail about different operating modes of 8255.
9. Discuss how to determine the control word for 8255.
11. Discuss the various operating modes of 8253.
12. Define Memory mapped I/O.
13. What is an interrupt I/O?
14. What are the two categories of an interrupt?
15. What is the purpose of an interrupt enable?
16. What is the size of ports in 8255?